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A single-mask substrate transfer technique for the fabrication of high-aspect-ratio micromachined structures

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Abstract

In this paper, a single-mask substrate transfer process for the fabrication of high-aspect-ratio (HAR) suspended structures is presented. The HAR silicon structures are fabricated using a deep reactive ion etching (DRIE) technique and then transferred to a glass wafer using silicon/thin film/glass anodic bonding and silicon thinning techniques. The HAR structures are released using self-aligned wet etching of the glass. Two key processes are discussed. One is the silicon/thin film/glass anodic bonding, with special emphasis on the effect of the bonding material on the bonding shear strength. The other is the silicon backside thinning via aqueous solution of potassium hydroxide (KOH). A lateral RF MEMS switch has been fabricated and demonstrates low loss up to 25 GHz. This substrate transfer process has the advantages of high-aspect ratio, low loss and high flexibility.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

A high-aspect ratio (HAR) is desired to provide sufficient lateral capacitance, to increase the sensitivity of the sensor and to suppress the out-of-plane motion for many microelectromechanical system (MEMS) devices and components, such as comb-drive actuators, inertial sensors and variable capacitors. There are mainly three types of fabrication processes for high-aspect-ratio suspended silicon structures. They are the SCREAM (single crystal reactive etching and metallization) process, the silicon-on-insulator (SOI) based process and the silicon-on-glass (SOG) based process.

In the SCREAM process, high-aspect-ratio structures are etched in a silicon wafer via reactive ion etching (RIE) technique, followed by the deposition of a thin layer of silicon dioxide (SiO_2). After removal of SiO_2 at the trench bottom, movable structures are released using silicon isotropic dry etching. Finally, metal is deposited [1, 2]. The SCREAM process only needs a normal silicon wafer and single mask to form suspended structures with thickness of 20 μm and an aspect ratio greater than 10. However, this process has two shortcomings. First, the etching depth varies with the trench width of the structures due to the aspect-ratio-depending-etching (ARDE) effect of the RIE or DRIE. Second, the release process sacrifices some of the silicon structures and results in an irregular shape at the bottom of the silicon structures. Both problems lead to the deviation of the mechanical performance of the device. The SOI-based process can avoid these problems. In the SOI wafer, the device silicon layer with uniform thickness is separated from the handle silicon layer by a buried oxide layer. After deposition and patterning of the hard mask, generally SiO_2, the device layer is etched via DRIE to form the high-aspect-ratio structures. Then, the movable structures are released using wet etching of the buried oxide or DRIE over etching [3, 4]. A glass substrate is more favorable than a silicon substrate for high frequency applications, such as radio frequency integrated circuits (RFIC) and RF MEMS devices, because of its low loss characteristic [5–7]. The

straightforward method to construct devices or circuits on glass is to first build RF circuits on a silicon wafer or a SOI wafer, and then transfer them to a glass substrate [5]. A bulk silicon dissolved wafer process is developed in such a way to fabricate 1–25 μm thick movable devices on a glass substrate, in which device structures are etched on a silicon wafer and are heavily boron doped, then the silicon wafer is anodically bonded to a glass followed by the silicon dissolving to leave heavily boron doped devices attached to the glass substrate [8]. However, it is difficult to fabricate thick MEMS structures using the silicon dissolved wafer process due to the limitation of the diffusion process. The typical diffusion time is 15–20 hours for a diffusion depth of 15–20 μm. In order to supply a thick device silicon layer (>30 μm) on the glass, the conventional SOG process is widely used [9–11]. In the conventional SOG process, some shallow trenches are etched in a glass wafer or the backside of a silicon wafer first. After the silicon wafer is anodically bonded to a glass wafer, the silicon wafer is thinned from the backside using either mechanical grinding/polishing or chemical etching with KOH. Then, the device structure patterns are aligned to the shallow trenches via a double-side alignment, followed by the formation of the high-aspect-ratio structures by etching through the silicon layer via DRIE process. However, the conventional SOG-based process has three shortcomings. First, the Si-glass stack always bows or warps after anodic bonding due to the residual stress of the bonding. Therefore, lithography resolution, double-side alignment and yield are restrained. Second, since the glass is a poor thermal conductor, the substrate temperature ramps rapidly during the DRIE process. Therefore, it worsens the DRIE etching quality of the high-aspect-ratio structures. Third, the notching effect is hash since glass is an insulating material. Low frequency ionization (380 kHz) in the high-density inductively coupled plasma (ICP) etch tool can reduce the notching effect by removing the accumulated charges on the insulating surfaces. However, when the etching depth is large (~100 μm) and over-etching lasts a long time, a notching effect damages the structures. To avoid the notching effect, a metal layer can be deposited and patterned on glass or on silicon before anodic bonding [11].

In this paper, a new substrate transfer process is developed to fabricate high-aspect-ratio silicon suspended structures with large thickness (>30 μm) on a glass substrate. This fabrication process is to first pattern the high-aspect-ratio silicon structure in desired shapes using the DRIE process. Then, the silicon structure is transferred to the glass substrate using a Si/thin film/glass anodic bonding process followed by two silicon thinning processes. Finally, the suspended structure is released by self-aligned etching of the glass. This fabrication process avoids all the problems in the conventional SOG-based process. The fabrication process flow is described in section 2. The two key unit processes—silicon/thin film/glass anodic bonding and silicon thinning using KOH etch are explored in sections 3 and 4, respectively. A conclusion is drawn in section 5.

2. Fabrication process flow

The substrate transfer fabrication process uses an 8 inch silicon wafer and a glass wafer to fabricate high-aspect-ratio suspended silicon structures on glass. The silicon wafer is 730 μm thick and has either low resistivity (ρ = 1–10 Ω cm) or high resistivity (ρ > 4000 Ω cm). The glass wafer is 500 μm–1 mm thick borosilicate Pyrex 7740 glass wafer. The process flow is shown in figure 1 and explained below.

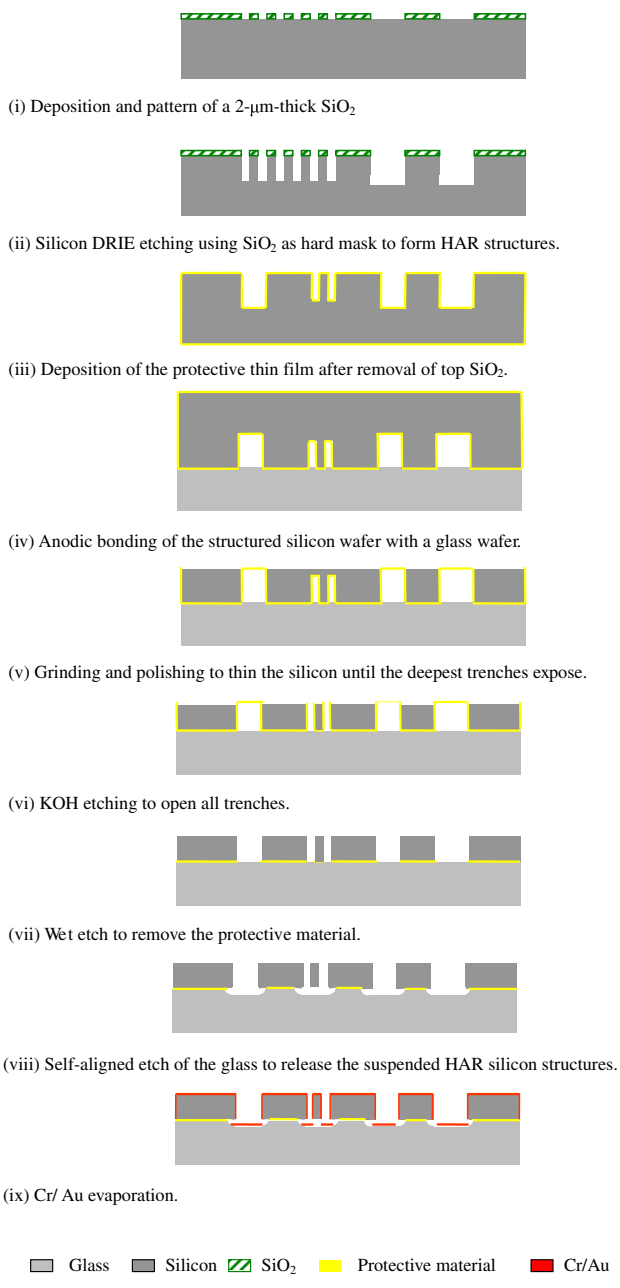


Figure 1. Schematic of the fabrication process flow.

(i) 2 μm thick SiO_2 is deposited using plasma enhanced chemical vapor deposition (PECVD) and etched using RIE.

(ii) Deep silicon trenches are etched using surface technology system (STS) high-density inductively coupled plasma (ICP) DRIE. The SiO_2 layer serves as the hard mask. The wide trenches are etched faster than the narrow trenches because of the ARDE effect of the DRIE process.

The aspect ratio is 30 for a 2 μm wide, 60 μm deep trench.

(iii) After removing the SiO_2 via RIE, all the exposed structures are covered with a protective thin film (thermal SiO_2 or silicon oxynitride (SiON)) in the furnace to prevent erosion of structures from KOH etching. Therefore, the protective thin film has to be resistible to the KOH solution and anodically bondable to the glass. The bonding shear stress has to be high enough to resist the subsequent grinding and polishing process.

(iv) The silicon and glass are anodically bonded together using Electronic Vision EV bonder EVG520 of EV group. The bonding temperature of 400 °C, voltage of 1000 V, piston force of 1800 N, chamber pressure of 3 mbar, and bonding times of 1 h and 30 min are used.

(v) The grinding process is employed to thin the silicon wafer rapidly using the GRIND-X GNX200 machine until the deepest trenches expose. The grinding rate is about 100 μm min^{-1}. Then, the polishing process is used to remove grinding marks and smooth the silicon surface. The polishing step sacrifices about 5 μm thick silicon. However, the grinding and polishing process cannot be used to expose all the structures directly since the brush and the slurry used in grinding and polishing process may damage tiny beams and block small trenches.

(vi) The stack is submerged in 35 wt% KOH aqueous solution at 40 °C to etch silicon until all the structures are exposed to the air. The wider trenches are opened first, followed by the narrower trenches. The protective thin film can prevent the erosion of sidewalls of the exposed silicon structures from the KOH solution.

(vii) The exposed protective thin film is removed using its respective wet etchant. For example, the thermal SiO_2 is etched by buffered oxide etchant (BOE) and the silicon oxynitride is etched by phosphorous acid.

(viii) The stack is dipped in the hydrofluoric acid (HF) solution for 30 min to etch glass and release movable structures. The silicon structures serve as the hard mask. Therefore, the glass etching is a self-aligned process. The concentration ratio of HF (49%):H_2O = 1:5 is used for smooth etching surface. After being rinsed in deionized (DI) water and dipped in isopropyl alcohol (IPA), the stack is dried using the critical point drying method.

(ix) A layer of metal may be optionally deposited using E-beam evaporation and covers the top surface and sidewalls of the silicon structures. A shadow mask can also be used to deposit metal at selective areas. This step is necessary only in designs that call for metal coating.

Figure 2 shows a SEM photograph of the cross-sectional view of a silicon trench fabricated using the proposed process. The straight silicon structure is about 50 μm thick. A cavity with sloping sidewalls is formed in the glass substrate after 30 min self-aligned etching. The vertical etching depth and the lateral undercutting are 5.7 μm and 10.2 μm, respectively. The lateral undercutting is nearly 1.8 times the vertical etching depth. Ideally, the isotropic chemical wet etching of glass should result in an undercutting equal to the vertical etching depth. The larger undercutting here could be due to the presence of a thin layer of native oxide (SiO_2) at the interface, which is formed during the anodic bonding. In HF solution, the native oxide is etched faster than the glass. The HF solution then moves laterally from the bonding interface to attack the native oxide, thereby increase the undercutting. 1000 Å chromium (Cr) and 1 μm gold (Au) are coated on the top and sidewall of the silicon structure uniformly. Due to the step coverage of the metal coating, the metal on the top is thicker than that on the sidewall.

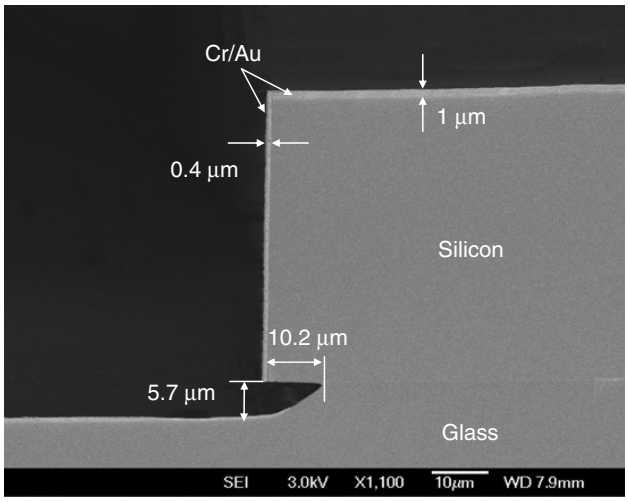


Figure 2. SEM microphoto of the cross-sectional view of a silicon trench after processing.

This single-mask substrate transfer process can provide high-aspect-ratio suspended structures on the glass substrate because the DRIE process is done on the bare silicon wafer. The notching effect, which always exists in the conventional SOG-based process, is avoided. The double-side alignment is also avoided since the suspended structures are released by glass self-aligned etching. Only one mask is needed. It is noted that the bonding quality of the silicon/thin film/glass anodic bonding pair is critical for this substrate transfer process as the bonding pair has to resist the subsequent grinding and polishing process and the KOH etching environment. For the silicon KOH etching process, the crystallography dependent etching may result in non-flat etching surface and the layout placement has to adjust to avoid it. These two processes will be discussed in the next two sections.

3. Si/thin film/glass anodic bonding

The basic setup of the anodic bonding process is shown in figure 3. The glass surface is placed against the thin film on the silicon surface. The sandwich is heated on a hot plate to 400 °C and a negative voltage of 1000 V is applied to the glass. Then, an electrostatic force is generated between the two wafers, resulting in an intimate contact of the bonding surface. The migration of ions creates an irreversible chemical bond at the interface. High electrostatic force helps strong bonding, and vice versa. When a thin film of dielectric material is coated on the silicon wafer, a portion of the applied voltage drops in the dielectric film and the other portion drops in the air gap. Therefore, the electrostatic force between the bonding surfaces is smaller and the bonding strength is weaker. When the thickness of the thin film increases or the permittivity of

Table 1. Tabular sample preparation and tested average shear force of anodic bonding.

Sample type	Resistivity of silicon (Ω cm)	Thin film on the silicon surface	Thickness of glass (μm)	Average shear force (kg)
A	1–10	–	500	6.8
B	1–10	SiO_2	500	5.7
C	1–10	SiO_2/SiN	500	0.66
D	1–10	SiO_2/SiN/SiON	500	4.6
E	1–10	SiO_2	1000	5.3
F	>4000	SiO_2	500	5.5

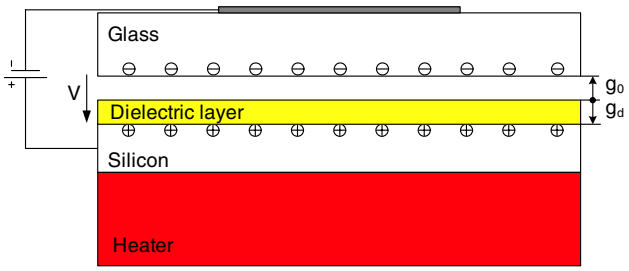


Figure 3. Schematic of the anodic bonding setup.

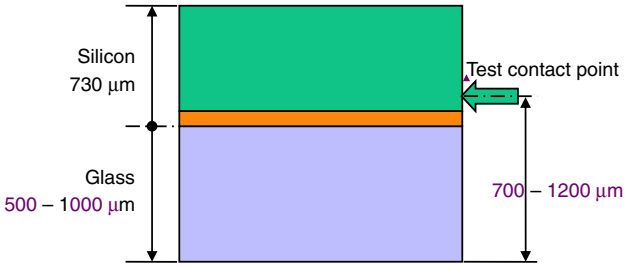


Figure 4. Schematic of the shear test setup.

the thin film decreases, the electrostatic force decreases further. The chemical reaction for the bond formation is also affected by the deposition of dielectric material due to the change of the bonding interface material.

Three process parameters are considered in this study. They are the material type of the thin film coated on the silicon wafer, the thickness of the glass wafer and the resistivity of the silicon wafer. In order to determine the effect of the various parameters on the bonding quality, six different anodic bonding samples are prepared, as listed in table 1. Sample A is a bare silicon wafer bonded with a 500 μm thick glass wafer. In Samples B–D, the silicon wafer is coated with different thin films. In Sample B, the silicon wafer is coated with 1000 Å wet thermal SiO_2. In Sample C, the silicon wafer is coated with 1000 Å wet thermal SiO_2, followed by 1000 Å silicon nitride (SiN) deposited using low pressure chemical vapor deposition (LPCVD). In Sample D, the silicon wafer is coated with the same thin film as in Sample C, and then is put in the wet oxidization furnace at 1000 °C for 1 h to oxidize the SiN surface to silicon oxynitride (SiON). In Samples E and F, the silicon wafers are coated with the same thin film as in Sample B. The glass wafer is 500 μm thick in Sample B and 1 mm thick in Sample E. The resistivity of the silicon wafer is less than 10 Ω cm in Sample B and more than 4000 Ω cm in Sample F. Same bonding conditions—the bonding temperature of 400 °C, voltage of 1000 V, piston force of 1800 N, chamber pressure of 3 mbar, and bonding times of 1 hour and 30 minutes, are used for all samples.

After the anodic bonding, it is observed that Samples A, B, D, E and F are bonded uniformly. All structures are bonded with glass. Some small colorful rings with diameters of less than 4 mm are at the bonding surface, which may be caused by incomplete cleaning. However, for Sample C, the bonding quality is relatively poor. Some bubbles with diameters of more than 3 cm are at the bonding surface of Sample C. Many small structures with feature size of less than 1 mm are unbonded.

To quantitatively evaluate the bonding quality, the tensile strength measurement is conducted commonly [12, 13]. The

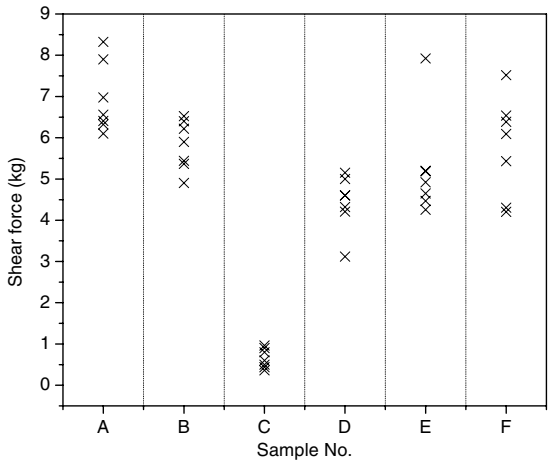
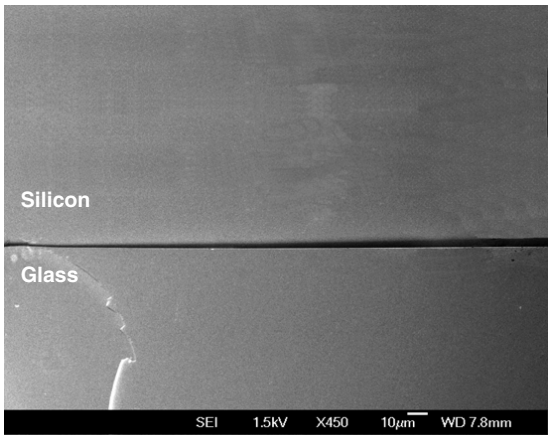


Figure 5. Plot of the measured shear force of different samples.

shear strength measurement has not been reported before. However, the shear strength measurement is relatively more important when the bonding wafers need to be ground and polished. Failure usually occurs when the external shear stress exceeds the limitation of the shear bonding strength. Figure 4 shows the schematic of the shear test setup using Dage Series 4000 Bond Tester. The glass of the bonding pair is faced down and the silicon is faced up. The shear height (the position of the test contact point) is set at 200 μm higher than the glass thickness. For instance, the shear height is set at 700 μm when the glass is 500 μm thick and 1200 μm when the glass is 1 mm thick. Every chip size is 2 mm × 2 mm. Seven test chips are prepared for each bonding sample. The bonding shear strength is represented by the shear force in the unit of kg. The experimental results of shear force are plotted in figure 5 and the average shear forces are summarized in table 1.

Thermal SiO_2 on silicon (Sample B) reduces the average shear force of the bonding pair from 6.8 kg (Sample A) to 5.7 kg. The deposition of 1000 Å SiN on thermal SiO_2 (Sample C) causes decrease of the average shear force to



(*a*) Sample C: SiO_2/SiN

(*b*) Sample D: SiO_2/SiN/SiON

Figure 6. SEM micrograph of the bonding interface region of the silicon/thin film/glass bonding pair: (*a*) Sample C and (*b*) Sample D.

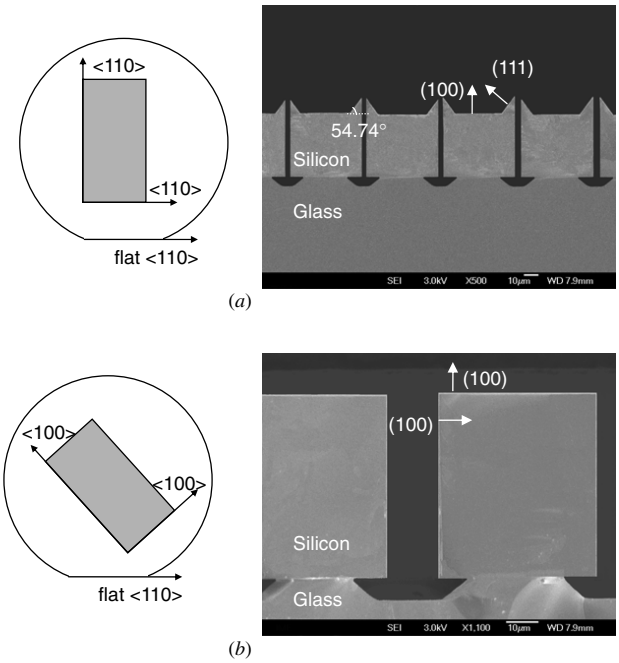


Figure 7. Schematic of the top view and SEM micrographs of the cross-sectional view showing the influence of the edge orientation on the silicon etching profile (*a*) 0° and (*b*) 45° to the ⟨1 1 0⟩ prime orientation flat.

0.66 kg. However, the wet thermal oxidization of the SiN to SiON (Sample D) increases the average shear force to 4.6 kg. This is lower than silicon/glass (Sample A) and silicon/SiO_2/glass (Sample B) bonding, but is much higher than the silicon/SiO_2/SiN/glass bonding (Sample C).

Figure 6 shows SEM photographs of the cross sectional view of Samples C and D to evaluate the bonding interface between the silicon and the glass. Figure 6(*a*) shows a distinct gap at the interface of Sample C, which means insufficient bond in Sample C (SiO_2 + SiN). However, when oxidizing the surface of SiN into SiON for Sample D, the bonding quality is improved abruptly, as shown in figure 6(*b*). In Sample D, the SiON layer is about 30 Å thick measured using a Rudolph ellipsometer. The refractive index of SiON on SiN is about 1.954 that is between the refractive index $n = 1.46$ of 1000 Å thermal SiO_2 and $n = 2.02$ of 1000 Å LPCVD SiN. This implies that the SiN surface has changed and some oxygen (O) atoms have reacted with SiN. In [14], it is found that the SiN film is highly dense and the surface terminates with Si–N bond. The Si–N bond is too strong to be broken at 400 °C. Therefore, the Si–O–Si bond cannot be formed in Sample C. However, in the 1000 °C furnace condition, the nitrogen in the SiN surface layer can be substituted by the oxygen, and then the thin silicon oxide (SiO_2)/oxynitride ($Si_xO_yN_z$) layer is formed. This layer contains a high density of H- and OH-groups at the surface, which helps the interfacial chemical reactions. Therefore, Si–O–Si bond can be formed in Sample D effectively and causes a strong bonding.

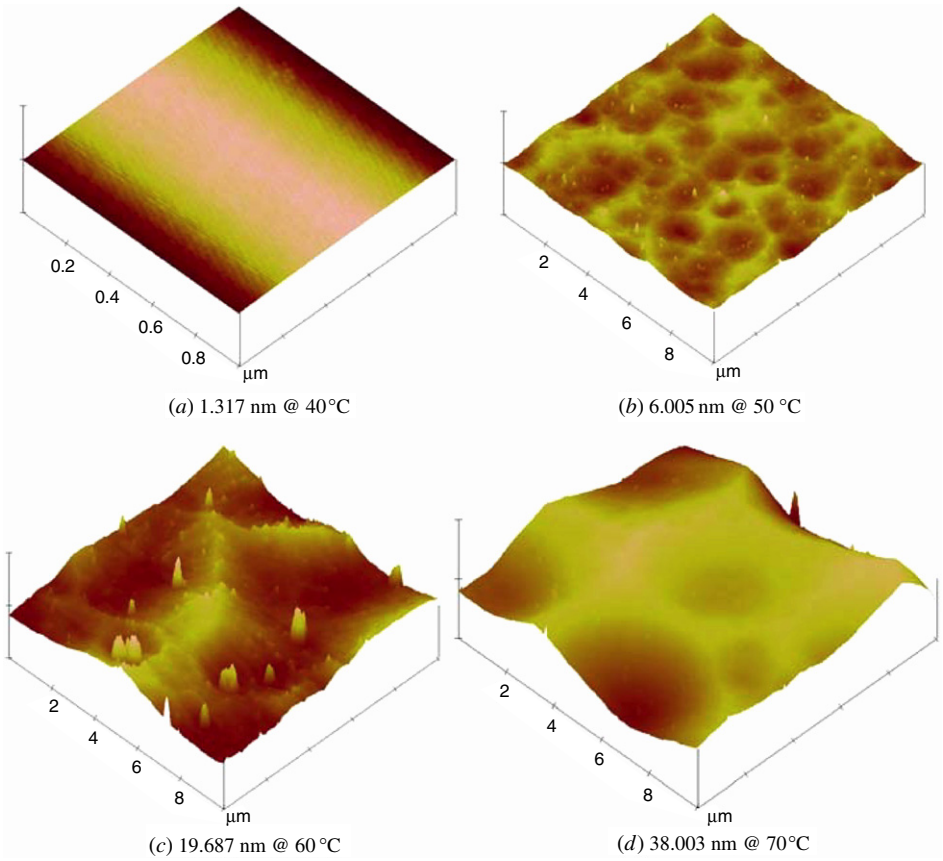
The average shear force of Sample E (1000 μm thick glass) is 5.3 kg, slightly lower than Sample B (500 μm thick glass), which implies the bonding strength is slightly weakened when the thickness of the glass increases. This is because thicker glass has larger electrical resistance, causing more voltage drop on the glass. Therefore, the effective voltage at the interface is reduced, resulting in a lower electrostatic force and weaker bonding.

The average shear force of Sample F ($\rho > 4000\ \Omega$ cm) is 5.6 kg, which is very close to Sample B ($\rho < 10\ \Omega$ cm). That means the resistivity of the silicon wafer has little effect on the bonding shear strength.

The experiment of the grinding process shows that the bonding quality of Sample C is so poor that the pair collapses during the grinding process. Other samples (Sample A, B, D, E and F) go through the grinding process successfully.

4. KOH etching for silicon thinning

The aqueous solution of KOH is used to thin the silicon wafer from the backside to expose all trenches in this process. The protective thin film, such as the thermal oxide and thermal oxide/SiN/SiON can provide effective protection to sidewalls of silicon structures. The experiment shows that the etching rate of the thermal oxide in 35 wt% KOH aqueous solution at 40 °C is approximately 300 Å h^{-1}, whereas the etching rate of LPCVD SiN is negligible. Therefore, the thermal oxide/SiN/SiON protective thin film is more effective when over-etching is long.



(*a*) 1.317 nm @ 40°C (*b*) 6.005 nm @ 50 °C

(*c*) 19.687 nm @ 60 °C (*d*) 38.003 nm @ 70°C

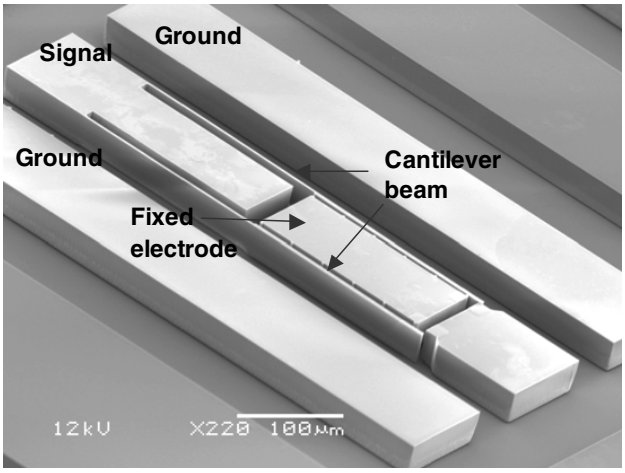
Figure 8. Surface roughness of silicon etched by 35 wt% KOH at different temperatures: (*a*) 40 °C, (*b*) 50 °C, (*c*) 60 °C and (*d*) 70 °C

The protective thin film can only protect sidewalls of structures from the KOH solution. The top surface is etched continuously. When the layout of the structures is designed arbitrarily, a V-shape groove may form on the top of the structures due to the silicon anisotropic etching characteristic in KOH solution [15]. Therefore, the layout design should consider the crystallography dependent etching of the silicon. In KOH etching, the {1 1 1} planes are extremely slow etching planes and are accepted to be the non-etching planes. Therefore, it is better not to expose them to the KOH solution so that the etching process can be controlled by adjusting the etching time and the etching surface can remain flat. The orientation plane that is introduced to KOH initially depends on the geometry and the prime orientation of the wafer. This study uses (1 0 0) silicon wafers with ⟨1 1 0⟩ prime orientation flat. When a rectangular wire is accurately aligned with the prime orientation flat, i.e. the ⟨1 1 0⟩ direction, only {1 1 1} planes are introduced as sidewalls from the very beginning of the KOH etching, which is 54.74° to {1 0 0} planes. In this case, the cross section of the etching pit is a V-shaped groove with ⟨1 1 0⟩ edges and {1 1 1} sidewalls, as shown in figure 7(a). There is one way to etch the silicon uniformly and produce vertical {1 0 0} walls on the structures. As shown in figure 7(*b*), the structures are aligned in such a way that the straight trenches are in 45° angle with the prime orientation flat (⟨1 1 0⟩ direction) of the (1 0 0) silicon wafer. There are {1 0 0} planes perpendicular to the wafer surface and their intersections with the wafer surface are ⟨1 0 0⟩ direction. Consequently, {1 0 0} facets are initially introduces as sidewalls. As both the bottom and the sidewall planes belong to the same {1 0 0} group, the lateral etching rate equals to the vertical etching rate. Hence, the exposed silicon can be etched vertically. The layout is turned 45° on the mask to accurately align straight wires with the ⟨1 0 0⟩ direction. However, the structure surface is not flat at the rectangular corner of the structure because tilted Si (1 1 1) walls appear. This effect can be reduced by minimizing the over-etching time and further optimizing the layout.

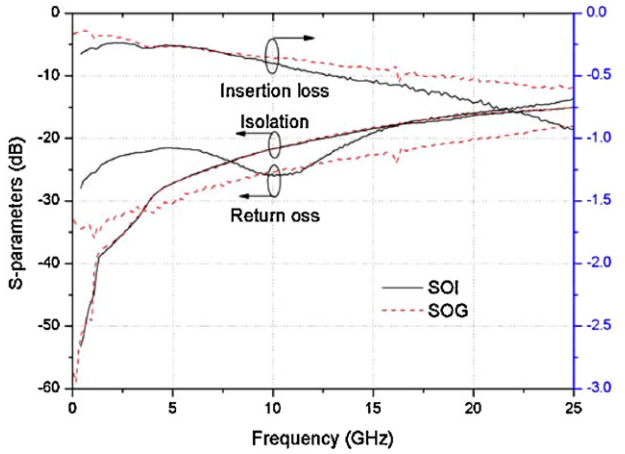
Table 2. The etching rate and surface roughness of silicon versus the etching temperature in 35 wt% KOH aqueous solution.

Etching temperature (°C)	Etching rate (μm h^{-1})	Surface roughness (nm)
23	2.95	–
40	12	1.317
50	29	6.005
60	40	19.687
70	62.4	38.003

KOH etching is a temperature dependent process, where the etching rate of silicon increases with the temperature. The etching rate of the silicon (1 0 0) in 35 wt% KOH solution is summarized in table 2. The stabilized etching temperature is ±2 °C. The etching rate is approximately 3 μm h^{-1} at room temperature and 62.4 μm h^{-1} at the temperature of 70 °C. However, surface roughness increases with the etching temperature too, as shown in figure 8. The roughness is



(*a*)



(*b*)

Figure 9. (*a*) SEM micrograph and (*b*) measured *S*-parameters of a lateral RF MEMS switch fabricated by SOI and our proposed SOG process.

measured using a Veeco AFM machine—Dimension 5000. It shows that when the etching temperature increases from 40 °C to 70 °C, the roughness of the etching surface increases rapidly from 1.317 nm to 38.003 nm. After the etching rate and the roughness of the silicon etching were taken into consideration, the silicon thinning of bonded wafer is carried out at 40 °C in 35 wt% KOH aqueous solution.

A low-loss lateral RF MEMS switch is fabricated using the proposed process. The SEM micrograph of the switch is shown in figure 9(*a*). It is an in-plane switch with two clamped-free cantilever beams. The beams are actuated by the electrostatic force once a sufficient bias voltage is applied between the cantilever beams and the fixed electrode. The gap between the beams and the fixed electrode is 4 μm, a little wider than that between the end point of the beam and the bumper, 3.5 μm. As a result, the cantilever beams hit the bumper first and do not strike the fixed electrode as actuated. The two cantilever beams are 2.5 μm wide, 470 μm long and 50 μm thick. The measured RF performance of the switch is shown in figure 9(*b*). It can be seen that glass substrate reduces the insertion loss of this switch by 0.4 dB at 25 GHz compared to the high-resistivity silicon substrate in the SOI-based process.

5. Conclusions

This paper presents a single-mask substrate transfer process for the fabrication of a high-aspect-ratio suspended silicon structure on the glass substrate. The process consists of the silicon DRIE etching process, the Si/thin film/glass anodic bonding, the silicon wafer thinning, the self-aligned glass etching and the metal deposition. Based on the study of Si/thin film/glass anodic bonding, the thermal oxide and the silicon oxynitride are chosen as the intermediate layer of the bonding, which can provide sufficient bonding strength with shear forces larger than 4.5 kg for the grinding and polishing process. In addition, these materials have strong resistant to KOH etching. The variation of the glass thickness and the silicon resistivity determines only slight changes in the bonding strength. Based on the analysis of the crystallography dependent etching of the silicon in the KOH solution, the device layout and the KOH etching conditions are optimized for the flatness and the smoothness of the silicon etching surface. A lateral RF MEMS switch has been fabricated and demonstrates low loss up to 25 GHz. The advantages of this single-mask glass-substrate process are low loss, high-aspect-ratio, high flexibility and low manufacturing cost. The potential applications include RF MEMS devices, comb-drive actuators, inertial sensors, etc.

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