Synthesized processing techniques for monolithic integration of nanometer-scale hole type photonic band gap crystal with micrometer-scale microelectromechanical structures

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This article reports the synthesized fabrication process design and module development that enabled the monolithic integration of deep submicrometer size, two dimensional hole-type photonic band gap crystals (PhCs) with microelectromechanical system (MEMS) actuators and optical testing structures (OTS). Techniques enabling sublithographic wavelength patterning using only conventional chrome-on-glass binary photomasks without phase shift features were achieved through the manipulation of mask bias designs and the partial coherence control of the lithographic exposure system. Together with the development of time multiplexed reactive ion etching and focus ion beam milling techniques, such design of the process allows the realization of highly dense PhC and MEMS actuators physically released from the buried oxide layer. Here, disparate pattern dimensions [with PhC critical dimensions (CDs) of only 175 nm, MEMS typical dimensions of 2 μm, and OTS openings more than 400 μm wide], varied etch depth (3 μm for the PhC and MEMS, 61 μm for the OTS), and the requirement of a sufficient process latitude for exposure and etch processes are some of the key challenges that were overcome for a successful integration of air-bridge-type PhC CDs with movable MEMS actuators. Hence, the works described in this article enable MEMS tunable PhC properties with potential application in next generation dynamic optical communication networks and photonic integrated circuits. © 2006 American Vacuum Society.

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I. INTRODUCTION

The fabrication of photonic crystals1 (PhCs) has been a field of intense study2 since the proposals3,4 of photonic band gap effect almost two decades ago. The challenges involved in the fabrication of superdense, periodic deep submicrometer size PhCs sensitive to optical wavelengths require critical dimensions (CDs) with periods of only a few hundred nanometers and even smaller linewidths. Such high density arrays of CDs have been a nontrivial challenge in fabrication even without the addition of other features,5,6 such as the introduction of tunability into PhC devices.7,8 Yet, worldwide research efforts to realize tunable PhC devices for applications with dynamic functionality,9 compensation of fabrication deviations, or modulation of signals10 in ultrasmall size optical integrated circuits11 remain intense. Mechanisms investigated for these purposes include temperature control,12 liquid crystal effects;13 material nonlinearity,14 optical tuning.15 and mechanical tuning mechanisms, of which, a microelectromechanical system (MEMS) tuning method16,17 has been identified to be suitable in the application to flip-state modulations where the inflection of states for dynamic PhC devices is enabled with switching times in the order of milliseconds.18 Hence, tunable PhC devices designed with MEMS would allow for an active control of PhC device output levels, useful in the application to next generation optical communication networks, and dynamic photonic integrated circuit devices. However, the incorporation of MEMS (Refs. 19 and 20) structures into PhC devices inevitably exacerbates fabrication challenges since MEMS fabrication by itself constitutes another set of special requirements21 in addition to those required by the nanometer-scale PhC structures.

The considerations necessary are as follows: To fabricate PhC devices operating at optical communication wavelengths centered about 1550 nm, the corresponding CDs required are in the hundred nanometer range. This requires not only the reduction of the optical lithographic wavelength from 365 nm i line to 248 nm, but also the ability of such deep ultraviolet (DUV) lithographic scanner systems to work at the sublithographic wavelength order. At the same time, because the ultrasmall CDs also shrink the process windows of all the other processing modules, especially in dimension sensitive reactions such as etching,22 advance fabrication techniques for each of these fabrication modules need to be developed.23

First, in patterning, albeit there are some other high resolution methods such as zone-plate-array lithography24 (ZPAL), electron beam lithography25 (EBL), holographic lithography26 (HL), and focused ion beam lithography...
(FIBL), DUV optical lithography\textsuperscript{27} (OL) was selected for development. This is because, although EBL (Ref. 28) is one of the most commonly used methods to define PhC patterns due to its ability to pattern arbitrary patterns at a very high resolution, it is affected by trade-offs between throughput and patterning flexibility. Such trade-offs in performance are also faced by the other methods such as HL and FIBL. While ZPAL is not constrained in this way, such systems are still not easily available. Therefore, in this article, the OL technique was chosen for development in application to the PhC with MEMS structures based on its inherent advantages of high throughput processing and also on its flexibility in exposure pattern type and density. Yet, the use of OL is fundamentally limited\textsuperscript{29} by its lithographic wavelength, and the diffraction limit defines the resolution of the smallest feature that can be patterned. Hence, for a predetermined lithographic wavelength system, further resolution enhancement techniques were developed to produce CDs smaller than the lithographic wavelength, using a method of pattern and partial coherence control.

Similarly, the challenges arising from the increased demand on CDs and reduced error tolerances\textsuperscript{30} are also encountered for other modules of PhC device fabrication, especially in etching and postprocessing. In etching, line edge roughness,\textsuperscript{31} etch lag,\textsuperscript{32} and notching\textsuperscript{33} effects, which has typical length scales in hundreds of nanometers to a few micrometers becomes critical to the successful fabrication of the hundred-nanometer-scale PhC CD structures. At the same time, the other processes of electrode metallization,\textsuperscript{34} and postprocessing buried oxide release\textsuperscript{35} (for air bridge PhC structures and movable MEMS actuators), also constitute challenges arising not only from the requirement of material compatibility\textsuperscript{36} and contamination control,\textsuperscript{37} but also from etch aspect ratio specifications\textsuperscript{38} and movable structure release stiction issues\textsuperscript{39,40}.

To present the details of this work in a sequential order, this article is organized as follows: In the first section, the technical rationale behind the designed process flow is given. The specific challenges addressed in each of the processing modules are presented in Sec. II. Specifically, Sec. II A describes the development of the subwavelength OL with resolution enhancements using only a conventional binary chrome patterned mask, while Sec. II B describes the issues of the resist deactivation for the chemical lithography developing process. Sections II C and II D go on to describe the etch fabrication of optical quality PhC structures without notchting damage. Finally, Sec. II E describes the modules for the integration of metallic electrode-annealing; postprocessing CD etching by focus ion beam (FIB) milling, and also the release of movable micromechanical structures without stiction or electrode peeling. In Sec. III, the results of the fabrication process designed and verified to enable the realization of deep submicrometer size tunable PhCs with MEMS comb drive actuators (comprising interdigitated comb fingers and folded suspension beam structures), released for mobility, are developed and presented.

II. PROCESS DESIGN AND MODULE DEVELOPMENT

The design of the process flow is a critical factor in the fabrication of PhC with MEMS structures not only for an effective development of each process module such that different requirements with corresponding recipes may be discovered through a rigorous design of experiments, but also for the proper sequence of processing steps to prevent the elemental contamination of reaction chambers, material degradations, process overruns, etc. Figure 1 depicts a schematic of the integrated fabrication process flow for PhC with MEMS structures, which may be described in four main parts: (I) film deposition for hard mask and electrode metallization, (II) PhC and MEMS comb drive CD patterning and transfer, (III) optical testing structure (OTS) fabrication aligned to the PhC device, and (IV) PhC etching and postprocessing.

Film material deposition processes were initiated with undoped silicate glass (USG) on cleaned silicon-on-insulator (SOI) wafers. Following an electrode pattern opening in hard mask [Fig. 1(a)], copper seed deposition and metallization plating [Fig. 1(b)] were carried out to enable the application of the MEMS actuation voltage. Planarization was then carried out using chemical mechanical polishing. To avoid contamination in subsequent steps, another layer of the USG film was deposited to cover the defined electrode [Fig. 1(c)]. The deposition of this protective USG layer therefore completes the first part of the thin film processes and lays foundation for the second set of steps necessary for a CD definition. Here, PhC together with MEMS comb drive structures were defined in photoreist on a layer of antireflection coating [Fig. 1(d)] prior to the magnetically enhance reactive ion etching (MERIE) of PhC for a good profile transfer of CDs onto the hard mask layer [Fig. 1(e)]. A complete resist strip after this step [Fig. 1(f)] in the second phase then allows the third phase of the OTS fabrication to begin.

Here, a different photoresist of higher viscosity was spun on thickly without first coating a bottom antireflection layer [Fig. 1(g)]. Due to the shallow depths of the hard mask patterns defined in the previous phase, the resist coating recipe may be developed to successfully planarize the surface, enabling the exposure of the second photomask after the alignment to at least five underlying marks patterned during the first exposure [Fig. 1(h)]. The testing structures exposed may therefore be sequentially etched for the hard mask oxide, SOI device silicon, SOI buried oxide, then SOI handle silicon again, till an etch depth of nearly 60 \( \mu m \) [Fig. 1(i)]. This step completes the construction of OTS, and the wafers undergo the final phase of PhC and MEMS actuator etching and other postprocessing modules.

In Fig. 1(j) photoresist stripping and polymer cleaning were performed prior to the device etching so as to enable a simultaneous etching of both PhC structures and the OTS using an etch recipe developed to optimize the etch quality of the PhC devices. After a device sidewall optimization, chemical buffered oxide etching (BOE) was then performed.
to release both the movable MEMS structures and the air-bridge-type PhC devices [Fig. 1(k)]. In this step, not only was peeling of the metallic electrodes prevented; precaution was also taken to ensure no further rework in case of contamination arising from the exposed electrodes. In Fig. 1(l), FIB milling was performed on released PhC air bridge structures to complete the process.

A. Pattern and partial coherence control for sublithographic wavelength critical dimension patterning without phase shift masking

In the optical lithography experiments, the CD of the smallest feature needed was less than the wavelength of the lithographic laser system. Such sublithographic wavelength
OL is diffraction limited, and special efforts are needed to enable a successful patterning. In the past, the most straightforward way to improve resolution was to decrease the wavelength of radiation, as illustrated in Fig. 2. However, the reduction of the wavelength beyond ArF lasers emitting at 193 nm would require a drastic redesigning of the lithographic system since shorter wavelengths are simply absorbed by the quartz lenses that direct the source light in current systems with laser wavelengths of 193–432 nm. Alternatively, resolution enhancement techniques (RETs) such as phase shift masking (PSM), optical proximity correction (OPC), and off axis illumination (OAI) may be used for exposure systems with specific wavelengths to improve their respective resolution limits [as indicated by the line marked with round symbols in Fig. 2(a)]. While each of these techniques improves base line resolutions, they are limited mainly by their respective drawbacks, which for PSM [Fig. 2(c)] and OPC are the cost and computational efforts required for implementation, while for the various OAI schemes illustrated in Fig. 2(b), it is the discrimination needed for varying pattern densities. Therefore, alternative approaches for achievement of subwavelength lithography resolutions have been widely investigated in recent years.

In this set of experiments carried out to achieve a sublithographic wavelength OL, only conventional binary chrome-on-glass photomasks of four times magnification without phase shift features were used. A positive DUV chemically amplified resist (CAR) Shipley UV210 was coated atop a bottom antireflection coating of Shipley AR3 using a Tokyo Electron ACT8 wafer-track system. A DUV Nikon S203B laser step and scan system was used for a controlled 248 nm wavelength exposure. The SOI wafers were first prepared using standard steps of cleaning, particle counting, and surface profiling before a blanket deposition of 5000 Å USG using a Novellus Concept Two Sequel plasma enhanced chemical vapor deposition (PECVD) system. The uniformity of the hard mask and other characterizations were then checked before the commencement of the lithography process.

Here, in the development of the OL process, it was a key consideration that out of the major components used in a set of optical exposure system, the radiation source cannot be easily changed as compared to the parameters of the condenser, mask, wafer, pattern design, resist chemistry, coating mechanisms, etc. The various parameters of the imaging system such as the lens set numerical aperture (NA) and the partial coherence of the condenser system design can also be varied for different lithographic performances. While an ideal lithographic projection tool should be coherent with a unity NA [a measure of how well a lens is able to collect diffracted light from a photomask and in turn project the
image onto the wafer as illustrated in Fig. 2(d)], real systems without an immersion technology cannot provide a unity NA nor a purely coherent illumination since the total image is the sum of all the intensity images from all source points. The degree of the coherence factor is usually expressed as

\[ \sigma = \frac{N_A_1}{N_A_p}, \]

where \( N_A_1 = n \sin \theta_1 \) and \( N_A_p = n \sin \psi_{\text{max}} \) represent the numerical aperture of the condenser and the projection lens, respectively which are in turn determined by the numerical aperture of the condenser and the projection lens, shown in Fig. 2, respectively. This equation not only provides the limits of OL as the image and condenser planes, respectively, but also indicates the latitude of process-derivation windows for different CDs. Hence, for 100, 200, and 300 nm linewidths by deep ultraviolet optical lithography. Therefore, an alternative control of the photomask pattern density and the lithographic partial coherence should be used to achieve such similar resolution improvements. For a partially coherent system, the resolution of the imaging system can be described with some correction to Eq. (2) such that

\[ R = k_1 \frac{\lambda}{(1 + \sigma)N_A}. \]

Therefore, the increase of the coherence factor can be used to derive improved resolutions.

Based on this, critical linewidth experiments may be carried out. An optimized resist coating recipe was applied, first with wafer surface priming by hexamethyldisilazane for an adhesion preparation, followed by a layer of AR3 that was spun at a combination of rotation speeds from 1.5 to 2.5 k rpm for 40 s before it was baked at 205° for 60 s. AR3 of 600 Å was then baked at 130° for 60 s. For the application of CAR with a thickness of 4800 Å, the resist was spun at rotation speeds from 1.5 to 4.5 k rpm for 40 s before it was baked at 205° for 60 s. AR3 of 600 Å was then baked at 130° for 60 s. For the application of CAR with a thickness of 4800 Å, the resist was spun at rotation speeds from 1.5 to 2.5 k rpm for 40 s. After a preexposure bake, the wafers undergo a wafer edge adhesion preparation, followed by a layer of AR3 that was primed with wafer surface for an adhesion preparation, followed by a layer of AR3 that was spun at a combination of rotation speeds from 1.5 to 2.5 k rpm for 40 s before it was baked at 205° for 60 s. AR3 of 600 Å was then baked at 130° for 60 s. For the application of CAR with a thickness of 4800 Å, the resist was spun at rotation speeds from 1.5 to 2.5 k rpm for 40 s. After a preexposure bake, the wafers undergo a wafer edge exposure for the removal of edge beads formed in the resist coating spiral stage (after about a thousand revolutions). Linewidth experiments were then carried out using patterns of lines with widths of 200 nm and duty factors (line/space ratio) of 1:3 and 1:1, as shown in Fig. 3. CDs of each set of duty factor experiments were taken using a Hitachi 9200 CD scanning electron microscopy (SEM) system. Based on an imaging system with a calibrated zero focus and a NA of 0.68, the designed linewidths of 200 nm were used in lithographic experiments for \( \sigma \) values of 0.38, 0.45, and 0.51. The results of the partial coherence variation experiments were plotted as measured CDs with respect to the exposure.
dosage used, as shown in Fig. 4. From the CD plots of the linewidth experiments, it can be seen that the 1:3 density patterns are much more sensitive to coherence factor variations than the 1:1 ones. Especially, the 1:3 density patterns have measured linewidths which were drastically reduced for the exposure with a coherence factor of 0.51 as compared to the exposures with coherence factors of 0.38 or 0.45. On the other hand, the higher density 1:1 patterns had similarly reduced linewidths for all three coherence factors used. From further such experiments, it was obtained that the reduction of original linewidths to less than 200 nm allowed for a further reduction of CDs obtained. However, such progressive reduction of design linewidths for the corresponding reduction of CDs approaches its limit at a drawn linewidth of 130 nm. This is due to the reduced process window of the smaller CDs, where small deviations in exposure and focus lead to lithographic failures.

Examples of typical exposure failures, brought about by such constraints, are shown in Figs. 5 and 6, where in Fig. 5(a), unresolved features result from an insufficient exposure dosage in spaces between dense line patterns, and in Fig. 5(b), resist peeling occurs at narrow ends of line patterns due to overexposure. In Fig. 6, there is the necking effect, where biasing of patterns near line terminations is required in order to prevent neck breakages at line ends. The layout and exposure lithographic variations are shown for a narrow line end [Fig. 6(a)], where there is the pull-back mechanism, and for a connected line end [Fig. 6(b)], where there is the flaring mechanism at the end of connected lines. Combined together, these two effects constitute the mechanisms for necking such that the pull-back mechanism coupled with flaring in the mild case leads to patterns of critical linewidths with constricted “neck” interfaces, as shown in Fig. 7(a). In the unbridled case of necking, extreme constrictions leading to critical line breakages at the line-base interface are shown in Fig. 7(b).

B. Resist poisoning in PhC lattice sites

A DUV radiation exposure on the CAR results in the formation of minute catalytic amounts of acids in the exposed
areas of CAR as determined by the openings on the chrome photomask. A subsequent processing by acid chemical-amplification processing then allows the CAR to become soluble in the alkaline-developer solution, allowing the removal of the exposed resist. If, however, the minute acid formed during the exposure is unintentionally quenched by base impurities on the wafer or in the environment, the chemical amplification can be deactivated, causing an erroneous patterning where CAR are not effectively removed by the developer where an opening should be. This type of “resist poisoning” is illustrated, for example, in Fig. 8 where a PhC lattice of holes was patterned and some holes are not properly developed to result in positions of missing holes. Such defects install optical states within band gap frequencies which can become microcavities that act as unintended resonators. To prevent the formation of such deactivated CAR, the presence of a weak base pyrimidine \( C_4H_4N_2 \) resulting from a treatment with a solvent should be avoided with a minimization of the resident time after the solvent cleaning process for a successful lithographic patterning. It is important to avoid such instances of resist poisoning since reworks are not only complicated but are also often ineffective.

C. Dense deep submicrometer critical dimension reactive ion etching profile control

To transfer the PhC patterns onto the device silicon, a MERIE recipe comprising a mixture of oxygen, argon, and carbonated fluoride chemistry was first used to transfer the CAR patterns onto the USG hard mask layer. After this, a surface technology system etcher with ICP sources for an independent control of plasma generation (coil) and biasing (platen) rf power was used to carry out the Bosch process, where time multiplexed etching and passivation processing allow for an abrupt application of reaction gases within the etch chamber. In this process, a silicon opening unprotected by a masking material is first etched using fluorinated gas chemistry comprising mainly of sulphur hexafluoride \( SF_6 \). Through the action of electron impact dissociation, reactive ions and ion-assisted fluorine radicals react with silicon openings to form volatile silicon by-product gases which are then removed to give an isotropic profile. This completes the etching phase, which is followed by the passivation phase, where octafluorocyclobutane \( C_8F_8 \) gas was applied as a protective polymer coating on both lateral and vertical surfaces. Repeated cycles of etching and passivation therefore constitute the time multiplexed scheme of deep reactive ion etching (DRIE). Especially, in such etching process, reactive etching species are directed onto the wafer surface with the assistance of high platen power biased in the vertical direction. Therefore, etching becomes much more significant in the vertical rather than in the lateral directions. Since the rate at which fluorine radicals are bombarded onto the horizontal surface far exceeds that of the vertical ones and passivation
In the experiments to develop DRIE conditions that allow the realization of the superdense PhC arrays, the coil power of the rf source was maintained at 600 W while the varied platen power was applied for the bias of ions energetic in the vertical direction, normal to the wafer surface. For a chemistry dominated by passivation, a slopped sidewall profile tends to result in gradually reduced etch openings that often result in eventual self-induced etch stops. Conversely, an insufficient passivation causes loss in anisotropy such that lateral etching increases to result in retrograde sidewalls. To avoid such sidewall profiles, etching and passivation process parameters can be delicately balanced in such high density deep submicrometer CD arrays to give conditions of sloped, retrograde, or vertical sidewall profiles, as given in the process parameters listing of Table II. Here, with time multiplexed reactive ion etching (TMRIE) listed in condition III of Table II, the etch profile of the CD structures can be moderated to obtain nearly vertical sidewalls, as shown in the cross sectional SEM of the etched PhC holes lattice in Fig. 9.

D. RIE lag and notching of PhC device at buried oxide interface

For etch patterns with different opening sizes, etch rates vary according to the effect of the aspect ratio resulting in the RIE lag. For etch openings of different linewidths, the etch rates vary drastically. This can be seen from the cross sectional SEM image of Fig. 10, where the most drastic difference in etch depth was obtained for the OTS structures with ultrawide etch areas, while for the thinner line patterns on the left, correspondingly increased etch depths were observed with progressively increasing linewidths. Such variations in etch rates with respect to aspect ratios and etch opening sizes arise as a result of several etch mechanisms, some of which include the ion and kinetic neutral shadowing effects, the transport of etch reactants toward and away from the etch surface, and the effect of electrical charges on the etch surface. One of the most prominent of these would be the transportation of etch reactants, which becomes progressively inhibited for narrower trenches. This is similarly so for the charge effect on the etch surface, where the charge distribution on the etch surfaces tends to be more highly concentrated in smaller etch surface opening areas than in larger ones. Hence, a higher charge density at the bottom of smaller

![Figure 8](image_url)

**Fig. 8.** (a) Cubic PhC hole array patterns with areas of resist poisoning (missing holes in uniform hole arrays). (b) Unintended resonators form within the PhC hole lattice.

### Table II. Etch and passivation time multiplexed reactive ion etching process parameters for various etch sidewall profiles of the sloped, retrograde, and vertical types.

<table>
<thead>
<tr>
<th>TMRIE conditions</th>
<th>Etch (SCCM)</th>
<th>Passivation (SCCM)</th>
<th>Co</th>
<th>Platen</th>
<th>Co</th>
<th>Platen</th>
<th>PhC etch profile</th>
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<tr>
<td></td>
<td>C&lt;sub&gt;4&lt;/sub&gt;F&lt;sub&gt;8&lt;/sub&gt;</td>
<td>SF&lt;sub&gt;6&lt;/sub&gt;</td>
<td>O&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Process cycle time</td>
<td>Power (watts)</td>
<td>C&lt;sub&gt;4&lt;/sub&gt;F&lt;sub&gt;8&lt;/sub&gt;</td>
<td>SF&lt;sub&gt;6&lt;/sub&gt;</td>
</tr>
<tr>
<td>I</td>
<td>30</td>
<td>1000</td>
<td>10</td>
<td>8</td>
<td>600</td>
<td>15</td>
<td>160</td>
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<tr>
<td>II</td>
<td>30</td>
<td>100</td>
<td>10</td>
<td>9</td>
<td>600</td>
<td>25</td>
<td>110</td>
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<tr>
<td>III</td>
<td>30</td>
<td>100</td>
<td>10</td>
<td>8</td>
<td>600</td>
<td>23</td>
<td>170</td>
</tr>
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Slopped
Retrograde
Vertical

trenches tends to result in the repulsion of incoming charged reactive species, which acts to reduce or even prohibit further etch actions eventually.

Such charge accumulation effect also comes into play in another circumstance—notching of the device silicon at the device and buried cladding oxide interface. This critical RIE effect is an important consideration in the SOI device etching. A SEM of this type of etch problem is as shown in Fig. 11(a). Here, there is a severe undercut of the silicon PhC near the bottom of the device, at the interface of the buried oxide layer. This is due to the accumulation of positively charged reactive ion etching species pulled down deep onto the etch surface by the vertical platen bias power. Such residual charge accumulation on the etch surface acts to deflect further incoming positive species when etching proceeds until the etch stop buried oxide charge insulating layer. This results in the lateral etching of the PhC structures near the device-cladding interface, as the etch species are deflected onto the sidewalls, as can be seen in Fig. 11(b). In the case of mild notching, the performance of the fabricated PhC structures would be adversely affected. However, if notching due to overetching was allowed to become extensive, then a total destruction of the designed device would result. To prevent this problem, this process was therefore designed as described in Sec. II such that only similar etch opening sizes and etch depths are required for each etch step. In this way, drastic etch lag effects would not result in the undercutting of larger etch features at the etch stop layer due to the overetching time required to complete the etching for the narrowest openings. Otherwise, the use of the periodic discharging technique to remove accumulated charges leading to sidewall deflected reactive ion etching (through periodic plasma discharging) is another tool related method to ameliorate notching effects.

E. Integrated metallization processing, air bridge, and movable structures released from buried oxide layer and etching on critical dimensions by focused ion beam milling

In the postprocessing process of the PhC, MEMS, and OTS devices, thermal oxidation was performed to improve the optical quality of device sidewalls through the smoothing of sharp facets. To enable the high temperature furnace process, a total strip of photoresist was necessary to avoid an organic contamination of the oxidation chamber. Through a wet clean recipe of piranha bath consisting of sulfuric acid ($\text{H}_2\text{SO}_4$) and hydrogen peroxide ($\text{H}_2\text{O}_2$) at high temperature of 130 °C, the polymers and remaining photoresist left over in the lithographic and etch process were removed and inspected under a defect review scanning electron microscope with energy dispersive x-ray analysis to ensure a complete stripping. The cleaned wafers were then oxidized in the furnace at 1050 °C for 90 min, consuming silicon at a rate of about 0.4 times the rate of oxidation. For oxidation of 1000 Å thickness, the sidewall edges of the time multiplexed DRIE etched sidewalls [Fig. 12(a)] are then rounded with reduced scallop depths [Fig. 12(b)]. Therefore, the optical quality of the fabricated device was improved and the optical scattering due to sidewall roughness was reduced.

Next, in the integration of electrode metallization for the MEMS comb drive electrodes, Cu seed deposition was first carried out using physical vapor deposition (PVD) for a conformal film of 250 Å tantalum (Ta) before the deposition of copper on top of the Ta layer which proceeded until a conformal coating was formed. Following the seeding, the actual
Cu film thickness required was then applied by electrochemical plating (ECP). In the plating cell, the Cu plating process was carried out with CuSO₄, H₂SO₄, and DI water solution baths. After plating, the wafer surface was cleaned by a DI water spray in the postplating module. Postannealing at 200 °C was then carried out before the Cu film was chemically polished to achieve the required planarized stack thickness and also to remove unwanted Cu over areas that should not be coated. This planarizing step therefore enables a subsequent processing of high resolution lithography after another USG deposition was carried out for cover over the metal electrodes (thereby preventing subsequent processing contamination). Upon completion of subsequent clean room processes, the defined Cu electrodes were exposed in the final phase using buried oxide etch (BOE) release which removes silicon oxide at a rate of 2500 Å/min. The wafers released with the wet etch bath (comprising ammonium fluoride and hydrofluoric acid) are then cleaned with DI water. For clean wafers spun dry at standard qualified recipe of 1800 rpm, peeling of the thinner metal electrodes with less area of adhesion to the underlying device silicon results. To prevent such defects, two approaches may be taken, namely, to reduce the spin speed of the dryer to 300 rpm or to alternatively allow the wafers to be evaporated dry after an isopropyl alcohol bath rinse (without undergoing spin dry). Although the latter method was more time consuming and less precise, its advantage over spin drying is the reduced likelihood for the occurrence of stiction (the permanent sticking of released movable structures).

Therefore, following the sidewall optimization and buried oxide release, the movable MEMS, PhC air bridge structure, and OTS were realized. A final FIB milling was then carried out on the CD of the PhC air bridge. Here, the FIB system uses liquid metal ion sources to form very small probes with high current densities. Where such high density ion beam...
strikes the required points on the silicon air bridge, silicon material was removed through a physical sputtering process. To carry out FIB milling on a CD structure, it was important that surface oxide was removed prior to the processing so that the effects of charging can be minimized for a sharper scanning electron imaging and therefore a more precise spatial milling. Optimized conditions were found for a magnification of 35,000 times and a beam duration of 8 s for each PhC hole milling. For higher order of magnifications used, greater imaging precision was adversely affected by the increased specimen charging effect that reduced the resolution of the PhC holes patterned.

### III. RESULTS AND CONCLUSION

A synthesis of fabrication processes, including deep UV lithography, time multiplexed RIE, structural release, and FIB milling on PhC CD structures, was realized to enable a monolithic integration of PhC optical structures with MEMS actuation devices. Figure 14(a) shows the fabricated PhC MEMS microactuators with the interdigitated comb fingers (supported by the folded suspension beam structures) together with the PhC air bridge CD structure and orthogonal OTS. Figure 14(b) shows the close up SEM of the air bridge structure with FIB milled PhC holes of 200 nm diameters, defined within a CD of 470 nm width. Here, for the folded suspension beam system, the displacement relationship of the comb drive with the voltage applied can be modeled as the force generated \( F_x \), being a ratio of the spring constant \( k_z \) of the suspension so that actuation is given as

\[
x = \frac{F_x}{k_z} = \frac{V^2(N t_{\text{beam}}/d)}{2E t_{\text{beam}}(BW/BL)}.
\]

where \( \varepsilon \) is the permittivity of free space, \( V \) is the voltage applied across the electrodes, \( N \) is the number of comb fingers, \( d \) is the gap distance between the comb fingers, \( E \) is the Young's modulus of silicon, \( t \) is the thickness of the structures, and \( BW \) and \( BL \) are the width and length of the suspension beams, respectively. Based on this model of the folded suspension beam comb drive structures, the simulated voltage actuation behavior is plotted as a smooth line in Fig. 15 where the abscissa plots the applied voltage and the ordinate plots the comb drive displacement distance. Also plotted on the same graph are the corresponding measurement results for the mechanical testing experiments, where the direct current voltage was applied to the electrode of the static comb while the ground potential was maintained on the electrode of the moving comb. Based on the captured images of the comb fingers at different applied voltages, the displacement distances for the various applied voltages were analyzed using image processing techniques to obtain the physical displacement values for each actuation voltage, which are then plotted as plus (+) symbols and connected by dotted lines on the graph of Fig. 15. A lateral instability was also monitored in the orthogonal direction using the same method and plotted with cross (x) symbols connected by dashed lines. As can be seen from the results of Fig. 15, the theoretical model describes the characteristics of the fabricated structures well in the actuation direction and reveals the limits of the operation till pull-in occurs, such that an effective voltage stability up to 20 V is determined. Other optical testing experiments for the PhC devices modulated by the movement of the MEMS actuator structures are still undergoing and will be presented in full detail in a future article.

To conclude, in the fabrication of tunable PhC with MEMS structures for disparate patterns and device etch depths, many techniques were developed to overcome the unavoidable challenges. The foremost include the design of a feasible processing flow that allowed for both PhC CD definition and etch together with actuator electrode metallization and also suspended released structures. Through the investigation of each process module to satisfy the demands of the device operating specifications (such as the PhC device operating at the canonical optical communication wavelengths and MEMS actuation voltage requirements, etc.), insights derived were applied to each module. In the first part of the process, an alternative method for the achievement of the sublithographic wavelength linewidth patterning, not commonly used in RETs such as PSM, OAI, and OPC, was de-
rived. Using low lithographic system requirements of a deep UV scanner working at a wavelength of 248 nm, chemically amplified photoresist coatings, and conventional chrome-on-glass photomasks, without expensive phase shift features or OAI systems, the sublithographic wavelength CDs were obtained using pattern and partial coherence control. Here, based on the key factors of pattern density bias and imaging system partial coherence variations, a smallest resolution of 36%, that of mask value, can be obtained for a resolution of 75 nm using a 200 nm binary photomask pattern. While the limit in the reduction of design linewidths and types of pattern together with constricted patterning at the line/base interface by line end necking are the limitations of this developed technique; the advantages of this method are its simplicity and cost effectiveness for the enhancement of the resolution without the use of an expensive PSM or high-end compensation computation technique, through simplified mask making requirements and a reduced demand on the exposure hardware sophistication. Such a derived method therefore may be used not only for PhC and deep submicrometer sized MEMS structures, but also for applications such as metal-semiconductor-metal photodetectors, nanoelectromechanical structures, etc.

At the same time, besides the description of the issue of resist poisoning in the patterning experiments, the etch lag effects and notching of devices at the interface of the silicon device and the buried oxide layer were also presented for the simultaneous implementation of PhC with MEMS actuators. The techniques of the FIB milling in the finalization step of the processing following the buried oxide release for PhC structures on CD structures enabled a wide processing window for both lithography and etch phases, avoiding severe loading effects caused by disparate pattern dimensions (such as etch lag and notching). Besides the realization of the deep etching TMRIE for the wide OTS grooves, PhC structures were also optimized through the delicate etch and passivation multiplexing balance and also through thermal oxidation. The effect of such fabrication process design not only addressed challenges arising from the need to incorporate structures with vastly different dimensional specifications, but also incorporates advantages of a batch processing capability with a manufacturing compatibility to other silicon devices. By a careful development of each experiment process module, a high resolution MEMS tunable PhC for use at an optical communication wavelength of 1550 nm was yielded such that a monolithically integrated tunable PhC was fabricated simultaneously with electromechanical actuators in mixed densities of superdense PhC holes, dense line patterns, isolated waveguide structures, and ultrawide OTS grooves that were defined as aligned to the deep submicron size PhC devices.

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