High resolution and aspect ratio two-dimensional photonic band-gap crystal

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This paper reports the challenges resolved to realize high aspect ratio pillar-type two-dimensional photonic band-gap crystal (PhC), designed for application at the optical communication wavelengths. Specifically, the issue of a drastically reduced process window of deep UV lithography and deep reactive ion etching, for a super dense array of submicron size pillars with a diameter of 230 nm and a spacing of 340 nm is treated. A rigorous design of experiments yielded high-resolution PhCs with precise lattice dimensions even near regions of “defect structures” designed for device operations. At the same time, in the etching process, the stringent requirement of an etch angle needed for successful realization of such a super dense array of submicron size PhC lattice was also satisfied to yield sidewalls of high verticality, aspect ratios greater than 50, and scallop-depths of 12 nm. © 2004 American Vacuum Society. [DOI: 10.1116/1.1819900]

I. INTRODUCTION

This article reports the progresses made to resolve fabrication challenges, for successful realization of high aspect ratio (HAR) two-dimensional (2D) photonic crystal (PhC) devices using deep UV (DUV) lithography and deep reactive ion etching (DRIE). The study of PhC structures has great potential for the development of lightwave circuits that utilizes photons instead of electrons for unprecedented processing speed and bandwidth—through manipulation of the photonic band-gap effect where light within band-gap frequencies cannot propagate. In other studies, the patterning of hole-type PhC devices on thin membranes with index guiding has by far been the mainstream technique investigated in the field. However, the pillar-type PhC structure remains as a critical study, for its high potential in demonstrating quantum level light manipulation. Yet, fabrications of such deep-submicron size pillar structures are fraught with difficulties. For instance, the definition of such a large array of small dimension features of pillars/holes with critical dimension of a mere few hundred of nanometers is not possible without the use of advance patterning tools such as electron beam lithography (EBL), focused ion beam lithography (FIBL), laser interferometric lithography (LIL), holographic lithography (HL), or deep-submicron wavelength optical lithography (OL). While EBL and FIBL are flexible, allowing definition of arbitrary patterns, they are sequential processes that can be inefficient for the definition of large array PhCs. In particular, EBL also poses additional stitching error implications. On the other hand, while LIL and HL are suitable for patterning with high efficiency, extended three-dimensional periodic structures, they are suitable mainly for regular patterns such that there are difficulties in patterning arbitrary “defect structures” where necessary. Hence, OL is a promising technique for 2D PhC definition due to its batch processing nature and also its ability to incorporate flexibility in the patterning of arbitrary defects. However, the feature size required of PhC applicable to the communication wavelengths has a critical dimension of 230 nm. This not only requires the reduction of optical lithography wavelength from 365 nm i-line to 248 nm but also the use of resolution enhancement techniques since the reduction of lithography proportional constants for improvement of resolution leads to problems of optical proximity errors, etc., affecting the performance of size sensitive PhC device structure adversely.

Similar to the situation of lithography, deep etching of small openings among a lattice of isolated pillar pattern involves many challenges. First, due to the reason that it is not a typical process (unlike that of hole-type PhC, which are like vias of integrated electronic circuits), there are relatively fewer studies that can be drawn on for reference. Second, even the choice of an etching method is limited for PhC devices due to the reason that precisely designed defect structures over a potentially large area, are necessary for fulfillment of unique device operation properties—take for instance the removal of a path of pillars/holes for waveguiding and the strategic placement of a tunneling defect for reduction of crosstalk at an intersection. Although macroporous silicon etch has been demonstrated to be capable of achieving HAR etch with good selectivity, it makes a demand on the doping levels of the silicon wafer and also faces challenges in achieving precise control of etched areas due to mask effects. FIB etch can be employed to perform etching in any direction without mask, but poses a similar efficiency problem as discussed above for EBL. Chemical assisted ion beam etching with pre-structured pores, though performs better than physical FIB, is limited by resistance of etch mask and ion beam deflection on sidewalls. Therefore,
electron cyclotron resonance (ECR) and inductive coupled plasma (ICP) etch may be used for etching in a direction perpendicular to wafer surface with a lower requirement in resistance of etch mask and wafer doping levels. However, due to the reason that ECR is a resonant technique, control parameters cannot be fully independent. At the same time, all time-multiplexed etch processes suffer from the formation of wavelike surface undulations that translate to surface roughness detrimental to optical performances. In addition, existences of sidewall angles that are typically negligible for larger dimension structures, are typically sufficient to cause total etch failures in the deep submicron length scale regime. Take for instance (see Fig. 1 for illustration), with a micro-electro-mechanical (MEMS) cantilever of 2 μm thickness, 10 μm depth and arbitrarily long length, an etching angle of 0.5 deg would result in an undercut of 87 nm on each facet. Therefore, the resulting width at the bottom of the beam would be 1.825 μm. However, for the case of a 200 nm diameter pillar, the undercut all-round would leave for a similar etch depth of 10 μm, a bottom diameter of only 26 nm. Such a weak base tends to topple the pillar, causing catastrophic etching failure.

Therefore, through carefully designed process flow, independent development of the lithographic and deep etching phases, together with integration of vastly different etching depths required are obtained as described in section two. Challenges of the OL process are addressed next in Sec. III, where the manipulation of lithographic parameters and also derivation of resolution enhancement model for optical proximity corrections (OPC) are achieved for DUV OL. Therefore, high-resolution PhC lattices are obtained, even for error prone regions near defect structures. The dense lattice of PhC pillars pattern with 230 nm diameter and spacing of 340 nm are then used for development of the deep etching formulations as described by Sec. IV. Here, besides yielding derivation of acceptable etch process window, very deep etching also allow for attaining of PhC lattices of HAR deep-submicron size pillars (aspect ratio beyond 50) previously unattainable by the DRIE method for such length scale. Together with the suppression of etch sidewall “scallops”—a critical shortcoming of time multiplexed etching—in the form of sidewall undulations causing surface roughness; an atypically low value of scallop depth, being only 12 nm was obtained. For the challenges that were addressed, the required PhC pillars may be applied to optical switching application in integrated optics for realization of nonblocking in-plane switching architecture or even the stopping and storing of light pulses coherently with an all-optical adiabatic and reversible pulse bandwidth compression process.

II. PROCESS DESIGN

To allow for independent manipulation of the lithographic and time-multiplex etch processes, different requirements for masking together with corresponding recipes are needed to realize drastically different mask openings and etch depths, for a PhC array of pillars (10 μm deep with 340 nm wide openings) and for deep trenches required to couple standard single mode fibers (more than 50 μm depth and 125 μm wide openings). A rigorous design of fabrication process such as that shown in Fig. 2 was used where an initial mask for the deep-submicron size PhC structures were first defined through a thin layer of hardmask. Photore sist strip can then be carried out for a refill of even thicker resist needed for fiber grooves etching defined using a second mask. When the
required depth of the fiber grooves are achieved, the photoresist may be stripped to reveal the PhC structures for device etch.

III. CHALLENGES IN DEEP-SUBMICRON OPTICAL LITHOGRAPHY

A. Lithography experiment set-up and methods

The lithographic experiments were carried out using a resist track; a deep UV scanner based on the Krypton-Fluoride laser of 248 nm and a binary mask of four times magnification without phase shift features with positive DUV resist (shipley UV210). Prior to resist coating, it is important that wafers are cleaned and primed to minimize the effect of surface oxides, which form long range hydrogen bonds with water adsorbed from air (resist adheres to water vapor rather than to wafer surface) resulting in poor resist adhesion to wafer surface. Therefore, in the experiments, cleaning and priming with hexamethyldisilazane (HMDS) was carried out using the liquid priming process of spinning solvent-diluted HMDS. Resist can then be spun onto primed wafer surface with the target of greatest possible uniform thickness. Although the physics of spinning is complicated, it can be determined to be strongly dependent on the evaporation rate of the solvent used together with the assistance of spin speed charts. A preexposure bake then drives solvent from the resist enabling high quality profile when appropriately carried out while decreasing the sensitivity of process if over-done. Post exposure, another bake is needed to reduce standing waves on resist profiles. Development of resist was then carried out following a final post-develop bake to improve the resist’s etch resistance.

B. Lithographic parameters manipulation

While the resolution of the lithographic process is not a fixed number but depends on the factors of pattern type, resist thickness, and wafer topography, it is generally easier to print an isolated feature than a dense pattern like that of a PhC structure. At the same time, it is important that the focus of a system is always checked and compensated for, prior to exposure by adjustment of lens to wafer distance. For projection method of lithography used, the “resolution” that determines the narrowest line/space of a repetitive pattern that can be correctly reproduced is given by

$$R = k_1 \frac{\lambda}{NA}$$

while the other critical factor, “depth of focus” is given by

$$DOF = k_2 \frac{\lambda}{NA^2},$$

where $k_1, k_2$ are process constants, $\lambda$ is the wavelength, and NA is the numerical aperture of the system. These factors effectively form the limiting determinants for the spread functions that control the size of isolated and dense patterns. When these parameters are not carefully controlled, typical failure modes that occur, include uprooted resist [Fig. 3(a)] due to diffracting wave misfocusing; missing patterns [Fig. 3(b)] due to illumination overdose and distorted shapes of resist profile [Fig. 3(c)] due to overlap wavefunctions interference.
According to Eq. (1), it is clear that for good resolution, the value of proportionality constant $k_1$ and $\lambda$ should be smallest possible while the value of NA is the largest possible. Technologically, the reduction of $\lambda$ hits a barrier beyond 193 nm since shorter wavelengths are simply absorbed by the quartz lenses that direct source light onto the wafer and therefore cannot be used without a drastic redesign of lithographic systems. At the same time, because the depth of focus (DOF) of Eq. (2) is inversely proportional to the square of the NA, increasing the aperture to improve resolution quickly decreases the DOF, which should have a value of greater than 500 nm since wafers cannot be perfectly flat and photoresist usually has thickness variation of several hundred nanometers. To increase the value of NA for better resolution, lens designs of larger diameters and greater lens element count are used to increase the amount of light collected through the photo mask. On the other hand, to reduce the trade-off between $R$ and DOF, $k_1$ can be reduced through improvement of the illumination coherence, antireflection coatings, and also resist parameters. Hence, two-level, multiple two factorial experiments were carried out by running the experiments with different levels of antireflection coatings and resist thickness to yield results of process windows summarized by the focus exposure matrices of Fig. 4.

From the plots, it can be seen that the poorest exposure latitude was obtained for the case of a high level of photoresist and low level of antireflection coatings [Fig. 4(b)] while an increase in the level of antireflection coatings still resulted in slanted profiles of the process window [Fig. 4(d)]. On the other hand, a decrease in the level of photoresist showed improvement in the latitude of process window for both high and low levels of antireflection coatings [Figs. 4(a) and 4(c)]. The plot of the focus exposure matrix with a low level of resist and high level of antireflection coating can be seen to yield the greatest exposure latitude and also focus range [Fig. 4(c)]. Hence, the effect of resist thickness can be significant and a smallest $k_1$ can be obtained for a lower level of resist thickness and higher level of antireflection coatings. These results supported the fact that reduced aberrations result from minimum resist thickness while the presence of antireflection coatings help reduce the effect of lithographic dimensional errors due to minimization of scattering from substrate material. Furthermore, it has also been identified that these two parameters have a minimum interaction effect.

Fig. 4. Plots of focus exposure matrix for (a) low level of resist thickness with low level of antireflection coating; (b) high level of resist thickness with low level of antireflection coating; (c) low level of resist thickness with high level of antireflection coating; and (d) high level of resist thickness with high level of antireflection coating.

Fig. 5. Dispersion characteristic of single line defect PhC waveguide (a) without, and (b) with optical proximity errors such that pillars near waveguide defects patterned much smaller.
as indicated by the nontwisting of their response surface when the results of Fig. 4 are plotted in three dimension.

C. Technique for enhancement of resolution

Beyond the improvement of Eqs. (1) and (2) as discussed above, other methods for resolution enhancement include techniques such as OPC, use of phase shift mask (PSM), and off-axis illumination (OAI) systems to manipulate the amplitude, phase, or propagation direction of the illuminating electromagnetic waves, respectively. While there are high computing powered programs available for OPC, these are often costly and in state-of-the-art integrated circuit (IC) layout tools. On the other hand, PSM is also relatively much more costly relative to a conventional binary photomask. Finally, while OAI of annulus, dipole, and quadrupole types had been demonstrated to work well for dense areas of repetitive patterns, the technique faces limitation for isolated features, which will often be encountered in our application to PhC device in the form of tunneling defects and the likes.

In this study, a binary mask and nonshifted axis illumination exposure system were used for achieving required PhC defect structures required within a dense matrix of otherwise similar sized PhC pillars. Here, the achievement of designed tunneling defect size is critical for successful fabrication of PhC devices with useful properties. A current challenge in this area lies in the fact that PhC devices are super dense arrays of periodic structures with feature size close to the lithographic wavelength. Hence, by the effect of diffraction, dense neighboring features illuminate to interfere with each other either constructively or destructively to print smaller and larger pillars, respectively, as opposed to being isolated, to give rise to the optical proximity error (OPE) effects. This unavoidable phenomenon affects the fundamental dispersion characteristic of a designed PhC drastically as can be seen in Fig. 5, in a single line defect waveguide where the pillars near the waveguide defects patterned much smaller than designed, such that the originally single mode waveguide becomes multimodal within the bandgap frequencies (Fig. 5).

To overcome this problem of OPE between bulk, semi-isolated structure, and isolated features, test patterns with mask biases of varying degrees and shapes were designed to yield critical dimension measurements for varying exposure energy \( E \), focus \( F \), “correction factor” \( CF \) and “shape factor” \( SF \). Here, CFs were varied with different sizes of the periphery PhC pillars and defined as their diameter ratio to that of the intended bulk pillars’ diameter as designed on the optical mask. The SF used corresponds to the circular and the square shape of the pillars drawn with width of squares equated to the diameters of the circular pillars needed (i.e., for the square shaped pillars drawn, the same definition of correction factor applies with simply replacement of square width with circular diameter). Based on these two designed experiment control parameters, the measured results are recorded as “experiment factor” \( EF \) giving the measured pillars’ diameter normalized by actual bulk PhC pillar diameter. For the two sizes of pillars diameters 300 and 360 nm investigated, two types of SFs (square and circular shape) and eight sets of CFs were tested using varying \( F \) and \( E \) between 0–0.2 and 18–22 mJcm\(^{-2}\), respectively. Each treatment combination of SF and PhC pillar size was varied against the other parameters as described to yield 43 sets of measurements each, resulting in a total of 172 data sets. By first studying the result of these experiments through scatter matrix plots, correlations of the experiment factors with respect to critical dimension errors measured can be deduced. Therefore, based on initial hypothetical multilinear models, with regressors of CF, \( E \), and \( F \) deduced accordingly, the OPE measured for the different structures can be used to obtain fitting parameters for each of the regressors such that prediction errors by the models are minimized. In this way, much-simplified OPC models were derived for both the semi-isolated and isolated structures, where the former was fitted with singular power factors of \( CF \), \( E \), and \( F \), while the latter was fitted with a double power factor for \( CF \) and singular power factor for \( E \) and \( F \). Thus, mask bias corrections can be made in anticipation of OPE, improving resolution of near sub-wavelength DUV OL without use of expensive PSM or high-end computations to yield compensated results of Fig. 6, where PhC device structures near defect structures
are obtained with desired dimensions.

IV. DEEP ETCHING PROCESS OF HAR DEEP-SUBMICRON SIZE Pillars

The patterned PhC lattice of circular resist islands on hardmask with high resolution as derived in Sec. III was transferred through a 500 nm thick silicon dioxide hardmask through a magnetically enhanced reactive ion etcher using a mixture of oxygen, argon, and carbonated fluoride chemistry to yield a DRIE etch hardmask.

A. Deep reactive ion etching method

Using a Surface Technology Systems (STS) deep etcher with ICP sources for plasma generation (coil) and biasing (platen), DRIE was carried out using the Bosch process where time multiplexed scheme of etching and passivation enabled by well-controlled gas inputs, facilitate the achievement of vertical sidewalls in deep etching that consumes relatively lesser protection material. This is due to the switching between etching and passivation steps that are repeated as necessary. First, a silicon opening unprotected by masking material is etched using fluorinated gas chemistry comprising mainly of sulphur hexafluoride (SF₆) to give a slightly isotropic profile (caused by lateral physical etch effect of impacting ions at etch surface). The action of reactive ions results mainly by the formation of ion and radical species, by electron impact dissociation so that the ion-assisted fluorine radicals then react with silicon openings to form a volatile silicon by-product gas, which is then removed. Here, by mixture of oxygen (O₂) in the etching gas chemistry, suitable sidewall passivation can be formed even during the etching phase such that the passivation layer derives from the formation of SiOₓ, which adsorbs onto the surface of exposed silicon as an oxide layer (with passivation properties since subsequent etching reaction requires its removal prior to action by F). Therefore, after the etching phase, the chamber is pumped out and passivation gas octafluorocyclobutane (C₈F₈) is applied for deposition onto the wafer (coating both base surfaces and also sidewalls of trenches and other openings).

These two steps are then repeated as necessary to obtain the required amount of etch and passivation cycling. Generally, due to the assistance of platen power for the vertical etch direction; the directionality of reacting ions in the vertical direction is high, compared to the rate at which fluorine radicals are bombarded onto laterally exposed surfaces due to impact scattering and also chemical reactions. Hence, the vertical etch component is much more significant such that the etch rate in the lateral direction is often considered negligible. At the same time, formation and removal of passivation compounds together with the etching of silicon must be designed to act in balance so as to maintain etch profile anisotropy. Otherwise, dominance by passivation would lead to low etch rates or even etch termination by surface residue.
build up. On the other hand, insufficient passivation leads to loss in anisotropy and extend of lateral etching increases.

**B. Unique considerations for HAR PhC pillars etch**

General RIE etch concepts that are established for standard micrometer size devices have to be applied with much more stringent requirements since reduction in feature size results in a corresponding decrease in process window and tolerance. Hence, due to the reason that PhC used at the optical communication wavelength of 1.55 \( \mu \text{m} \) has the critical dimensions of only a few hundred nanometers, stepwise isotropy and lateral etch rates need to be carefully monitored to prevent fabrication failure as described above by Fig. 1.

At the same time, etch scallops of undulations in sidewalls are inevitably formed during the etch/passivation cycling process due to the existence of isotropy in etch species bombardment phase. Past results of DRIE (Ref. 25) has demonstrated scallop depths ranging between 50 and 300 nm. However, such depths of undulations on PhC pillars can be unacceptable, as diffused scattering caused by such drastic scalloping can obliterate precisely designed Bragg reflections (off the designed PhC lattice structure) that constitutes the photonic band-gap effect. Therefore, to ensure that PhC properties are preserved, it is important that etch scallop effect resulting in the etch profile undulations be kept at a minimum to reduce the effect of diffused scatterings.

**C. Development of DRIE**

Here, the time multiplexed action of etching and passivation gases applied with independent bias control of the substrate was studied using an initial recipe of manual pressure control at 50%; etching chemistry comprising of C\(_4\)F\(_8\), SF\(_6\) and O\(_2\) gases, and passivation chemistry comprising only the C\(_4\)F\(_8\) gas. The coil power was maintained at 600 W for both passivation and etch phase, while platen power was applied only for the etch phase. For dominating passivation process, a reentrant etch sidewall profile was obtained with a lower etch rate, often resulting in self-induced etch stops. This is due to the reason that plasma polymerization reactions require relatively high ion bombardment energies of several hundred electron volts for their complete removal. At the same time, besides termination by surface residue built up, dominance of passivation also results in the incomplete removal of passivation component that leads to the formation of grasslike residues that is commonly known as “black silicon” (Fig. 7). Conversely, insufficient passivation causes loss in anisotropy such that lateral etching increases to result in the PhC pillars being severed (Fig. 8). Often, such lateral etch effect can easily take dominance with the small diameters of the PhC pillars, such that pillars severed along their length leads to “runaway etching,” such that the etch openings become extended and etch species take over etching in the entire area that was previously filled with pillars to result in a “released hard mask” situation (Fig. 9).

To overcome such undesirable defective etch situation, etching gas flow rates and durations can be reduced while the corresponding values increased for the passivation phase. At the same time, other methods of reducing the dominance of etch include the decreasing of chamber pressure and also the platen power applied. Such processes and their respective parameters are compared in Table I. Therefore, through balance of etch and passivation dominance and a reduced platen power, an acceptable process window for survival of deep-submicron size pillars can be found, based on an etch chemistry of SF\(_6\) (100 sccm), C\(_4\)F\(_8\) (30 sccm), and O\(_2\) (10 sccm) at pressure of 50% using platen power of 23 W together with a passivation chemistry of C\(_4\)F\(_8\) (160 sccm) at the same plasma power but without application of platen bias to yield results of Fig. 10.

### Table I. Process parameters of DRIE processes.

<table>
<thead>
<tr>
<th>Processes</th>
<th>Gas flow (sccm)</th>
<th>Power (watts)</th>
<th>Process cycle time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C4F8 SF6 O2</td>
<td>Coil Platen</td>
<td></td>
</tr>
<tr>
<td>Condition i</td>
<td>30 100 10</td>
<td>600 23</td>
<td>8</td>
</tr>
<tr>
<td>Re-entrant</td>
<td>Etch</td>
<td>Passivation</td>
<td></td>
</tr>
<tr>
<td>profile</td>
<td>160 0 0</td>
<td>600 0</td>
<td>5</td>
</tr>
<tr>
<td>Condition ii</td>
<td>30 100 10</td>
<td>600 23</td>
<td>9</td>
</tr>
<tr>
<td>Lateral</td>
<td>Etch</td>
<td>Passivation</td>
<td></td>
</tr>
<tr>
<td>dominant</td>
<td>110 0 0</td>
<td>600 0</td>
<td>5</td>
</tr>
<tr>
<td>Condition iii</td>
<td>90 40 0</td>
<td>800 20</td>
<td>-</td>
</tr>
<tr>
<td>Continuous</td>
<td>Etch</td>
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Fig. 10. Surviving PhC pillar array, without catastrophic fabrication failures but with rough sidewalls due to etch scallops undulations.
As can be seen, although surviving PhC pillars are obtained, the sidewall profiles of this etch process has rough surfaces due to large undulations arising from etch scalloping effect. Here, it can be measured from cross-sectional scanning electron micrograph that the scallop depth is 106 nm while the scallop height is about 150 nm. Intuitively, removal of etch-passivation cycling in DRIE process should result in minimization of sidewall scallops. However, it was found that although a continuous etch with plasma polymerization yields consistently smooth sidewalls, it was achieved at the expense of isotropic sidewall angles leading to lateral under cutting, which once again led to etch failures of Figs. 8 and 9. Therefore, to optimize the recipe for reduction of scallop depths so as to achieve smoother sidewalls, a further reduction of etch isotropy was carried out to balance both reduction of etch dominance and increase in etch duration. Based on this principle, tremendous improvement in sidewall etch profile was indeed obtained as can be seen from Fig. 11, where scallop depths of only 12 nm was obtained for a drastic improvement from an initial 106 nm.

At the same time, from the experiments, it was found that contrary to conventional assumption that lateral etching of DRIE structures are negligible beyond typical scalloping effects, progressive etch durations of deep-submicron size pillars (unlike for larger structures) consistently resulted in upper pillar critical dimension reductions. Therefore, it can be deduced that the size reduced geometries resulted in a significant action of etch on structures near wafer surface. Such phenomenon can be attributed to the trapped nature of the etch species along the narrow etch paths that results in sidewalls being further etched laterally. Consequently, incorporation of mask design bias in addition to that for OPC derived in Sec. III is required for successful realization of targeted devices.

V. CONCLUSION

Based on identified advantage of batch processing in optical lithography and DRIE, insights into the optimization of these techniques have been presented. Here, simplified models for OPC were derived heuristically for both semi-isolated and isolated defect structures, allowing for enhancement of resolution without use of expensive PSM or high-end compensation computation technique. At the same time, experiments of DRIE revealed many interesting effects, which were previously unemphasized since they were quite negligible for larger dimensioned structures (such as that of the amplified etch angle; process time effect on lateral etch, and sidewall scallops, etc.). By careful consideration of such experimental effects, HAR deep-submicron size pillars of PhC for use at communication wavelength of 1.55 μm as shown in Fig. 12 were yielded. The HAR pillars (aspect ratio 45–57) with small scallop depths (12 nm) are the deepest and smoothest by far achieved by DRIE technique used in this length scale.
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